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COLLINS RADIO

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Packet Radio Temporary Note #128

Packet Radio Station Interface

PACKET RADIO STATION INTERFACE

1.0 GENERAL DISCUSSION

The ARPANET Host-Imp interface as described in BB&N Report No. 1822 will be implemented as the Packet Radio Unit Station Interface. This is a bit serial interface that is symmetrical for transmit and receive. A discussion of the implementation of this interface is included here. Exceptions and rules of use are included where they have been recognized.

1.1 Characteristics

Maximum Data Rate:	One megabit/sec. The data rate is a function of the associated station CPU interface system and hardware requirements. Independent Adjustments are provided in the PRU for slowing down both the receive and transmit data rate by inserting a delay of up to 10 μs in the handshake paths.
Data Transfer:	Full duplex.
Signalling:	Bit asynchronous with request/ acknowledge per bit.
Interface Output Levels:	Differential line drivers/receivers. Twisted pair transmission line with nominal impedance of 120 ohms. (See Section 5 for Electrical Interface Details).

1.2 Exceptions and User Rules (Refer to BB&N Report No. 1822)

Word Boundaries:	Data transferred across the interface will always end on 16-bit word boundaries. The last host bit must occur on the 16th bit of a word. The packet radio's CPU will not fill out the last word with zeros.

1.3 Four-Way Handshake

The interface will be designed to operate in the 4-way handshake mode and will not operate in the two-way handshake mode.

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1.4 Additions

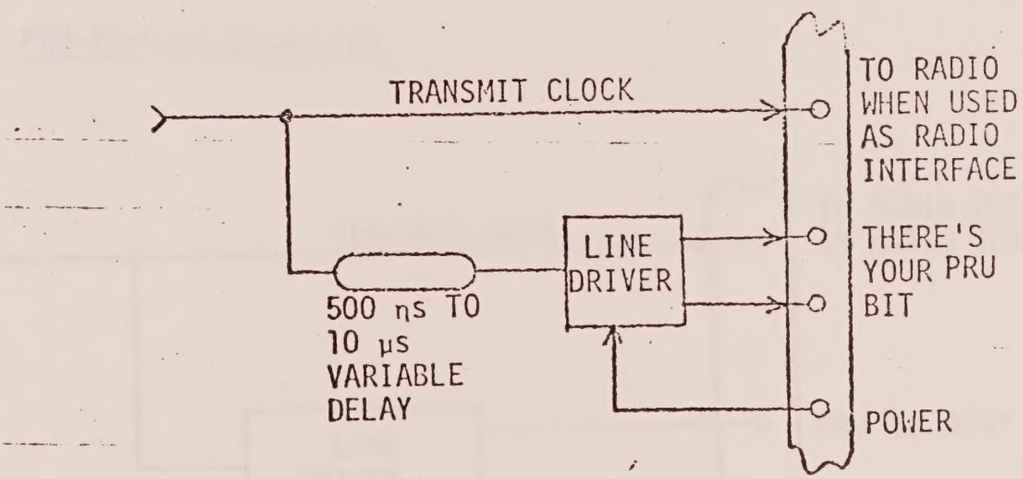
This interface has potential "hang-up" modes that could be disruptive to normal service. Since each receiver asks for data (READY FOR NEXT BIT) and waits for the response from the transmitter (THERE'S YOUR NEXT BIT), each could become "hung" due to a fault condition. To allow recovery from these fault conditions, a hardware timer (approximately 1 millisecond) will be added to both the transmit and receive interface circuits at the PRU CPU. This timer will detect when a data exchange stops before completion and interrupt the PRU CPU. The timers are not enabled until the start of a packet transmission. No status lines other than the PRU ready relay exist to tell the station CPU that this time-out has occurred.

2.0 TRANSMIT INTERFACE

Described below are the signals used to send data from the PRU to the host processor interface. The relationship of these signals and those defined for the PRU/RADIO are shown since one transmit interface board to serve both purposes will be designed.

2.1 There's-Your-PRU-Bit

This signal looks essentially like transmit clock in the digital/radio interface with the exception that data must be valid 500 ns before There's-Your-PRU-Bit is raised. The addition to the transmit interface board to generate this function will be:



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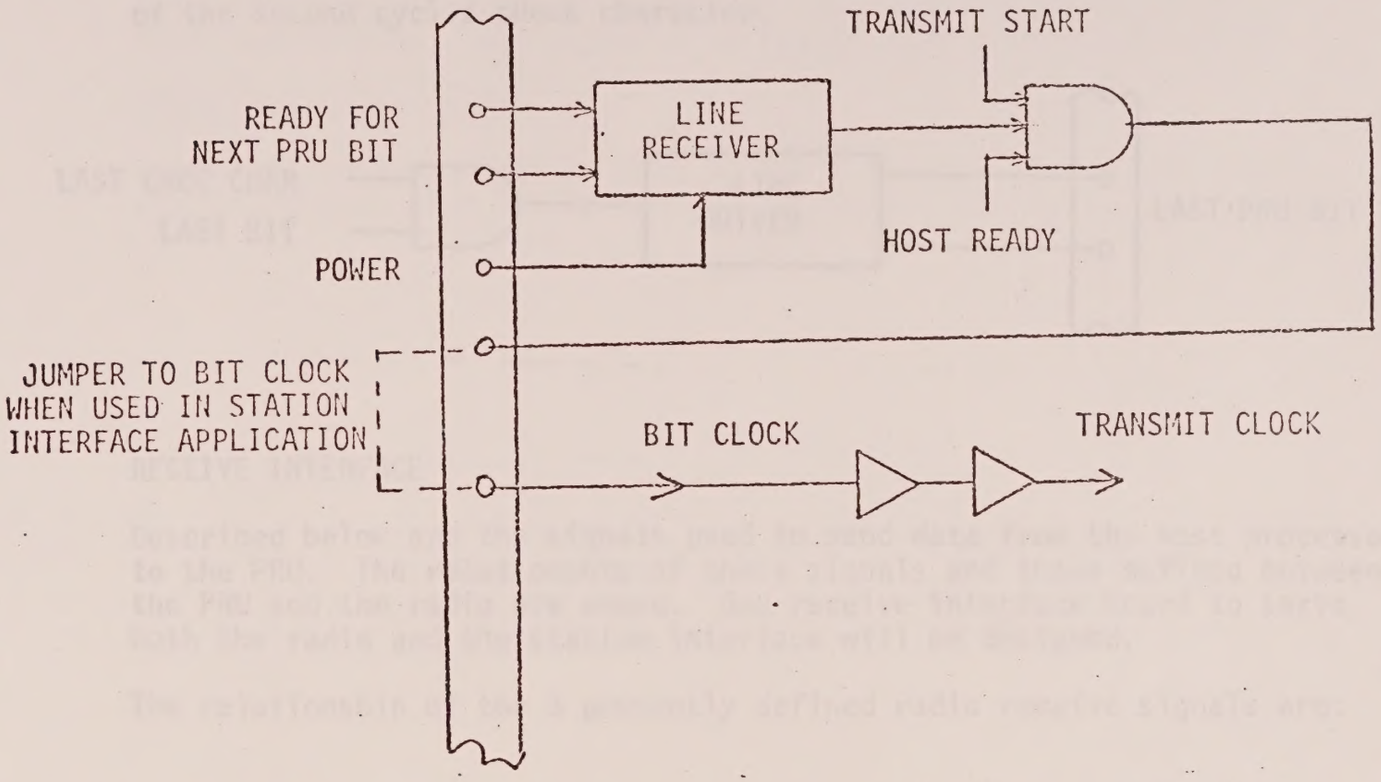
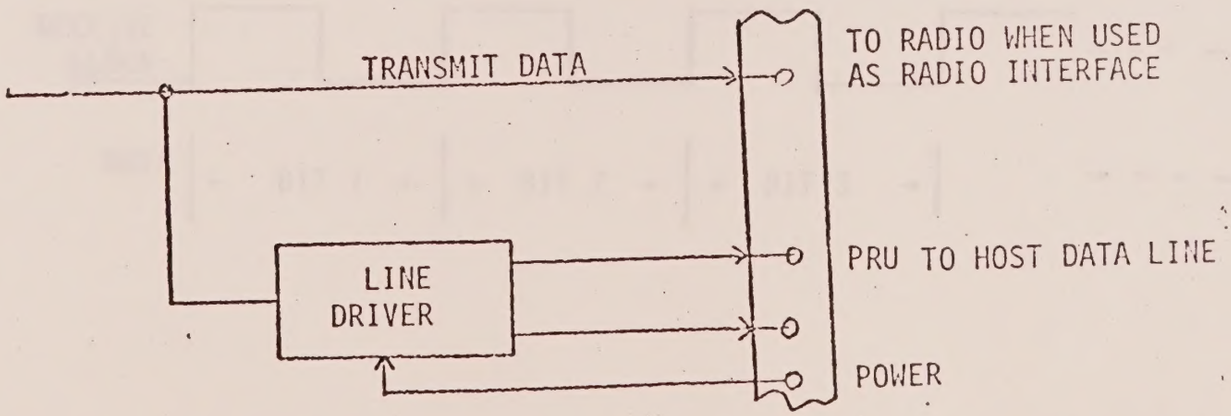
2.2 Ready-For-Next-PRU-Bit

Except during start-up, this signal looks like the bit clock received from the radio. Gating this signal with TX start, which is a signal within the transmit interface board that goes true when the interface is ready to receive clock and providing a 500 ns deskewing delay, will allow Ready-For-Next-PRU bit to be used as bit clock.



2.3 PRU-To-Host-Data-Line



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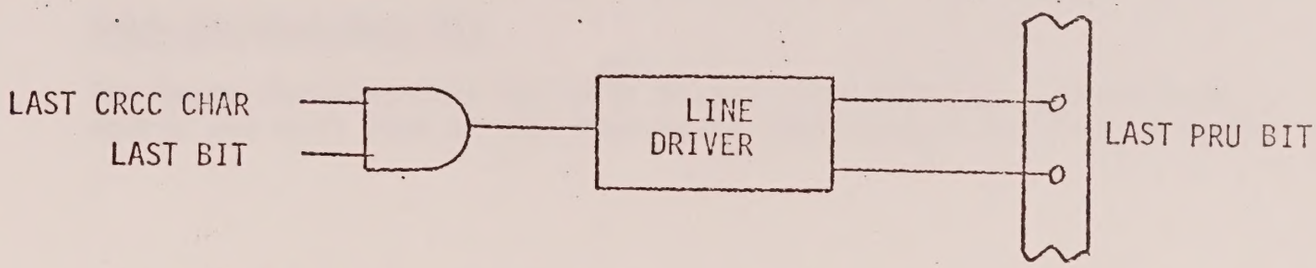
2.4 Last-PRU-Bit

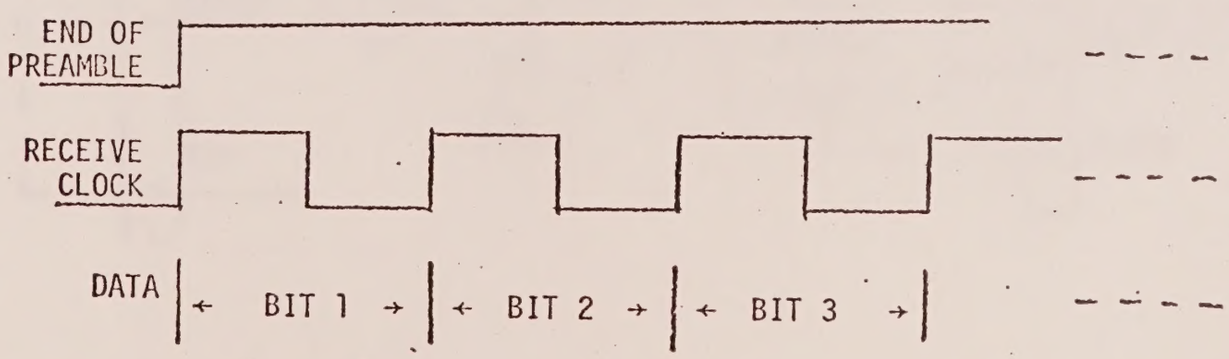
The last PRU bit will be generated by anding the "last cycle check character state" with the 16-bit signal to generate the Last-PRU-bit. Using this timing means that the last two words (32 bits) of the transmission, before Last-PRU bit goes true, will be the cyclic check character words. The Last-PRU bit will be true during the last bit of the second cyclic check character.



3.0 RECEIVE INTERFACE

Described below are the signals used to send data from the host processor to the PRU. The relationship of these signals and those defined between the PRU and the radio are shown. One receive interface board to serve both the radio and the station interface will be designed.

The relationship of the 3 presently defined radio receive signals are:



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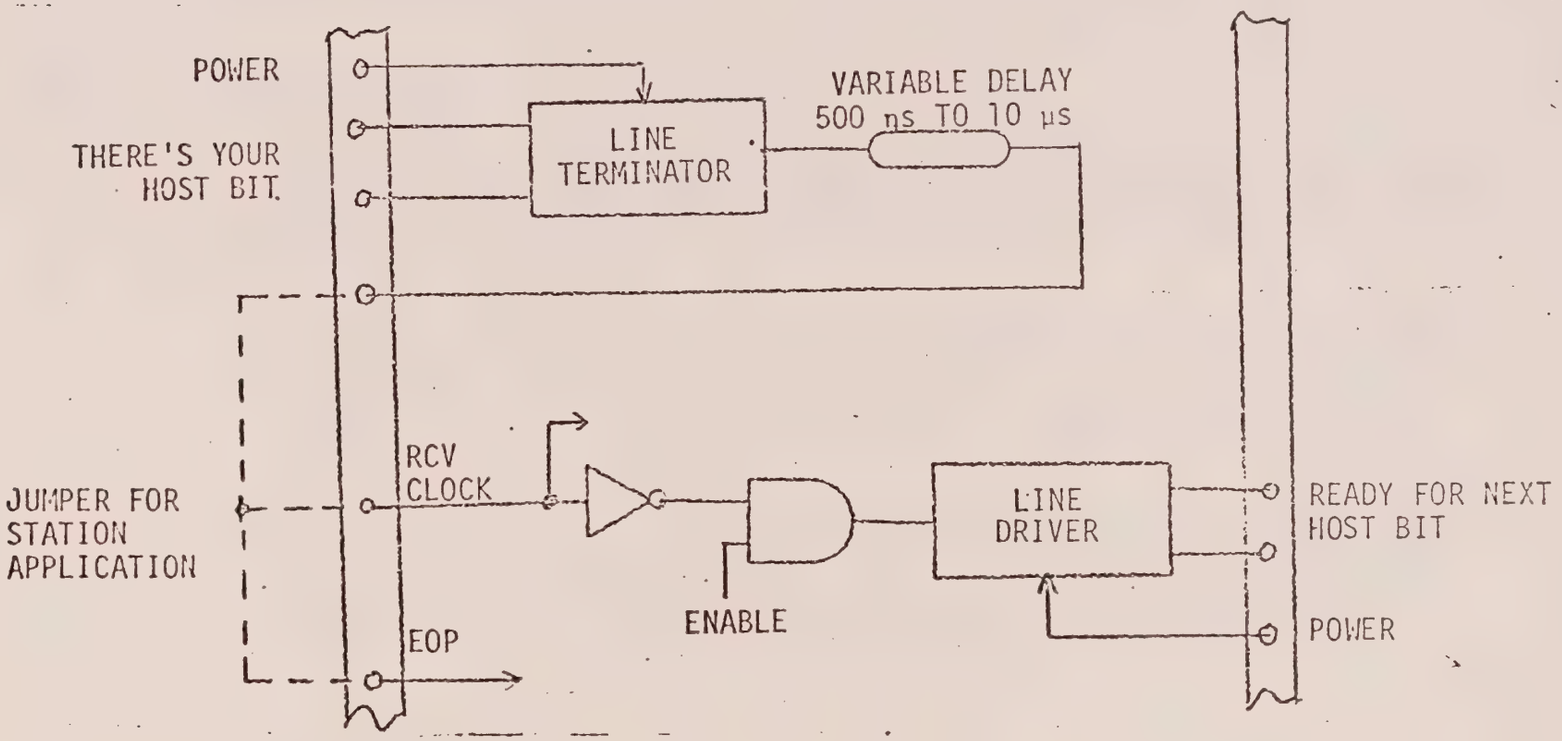
3.1 There's-Your-Host-Bit

This signal will be delayed 500 µs to allow for skew with the data bit and will be fed into the receive clock signal input. It will also be fed into the End of Preamble (EOP) input. Since this input now senses the leading edge of EOP to set a flip flop, sensing the leading edge of There's-Your'Host-Bit will cause the flip flop to set on the first bit, resulting in identical timing to the presently defined radio interface timing. This signal will not be sent without HOST-READY.

3.2 Ready-For-Next-Host-Bit

The Ready-For-Next-Host bit will be set high when the program sets enable and will then be the inverse of There's-Your-Host bit delayed:



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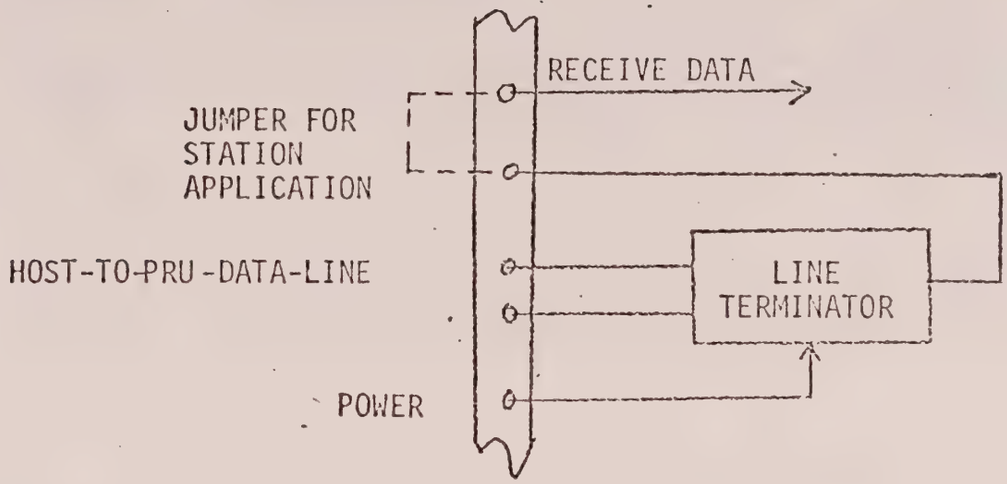
3.3 Host-To-PRU-Data Line

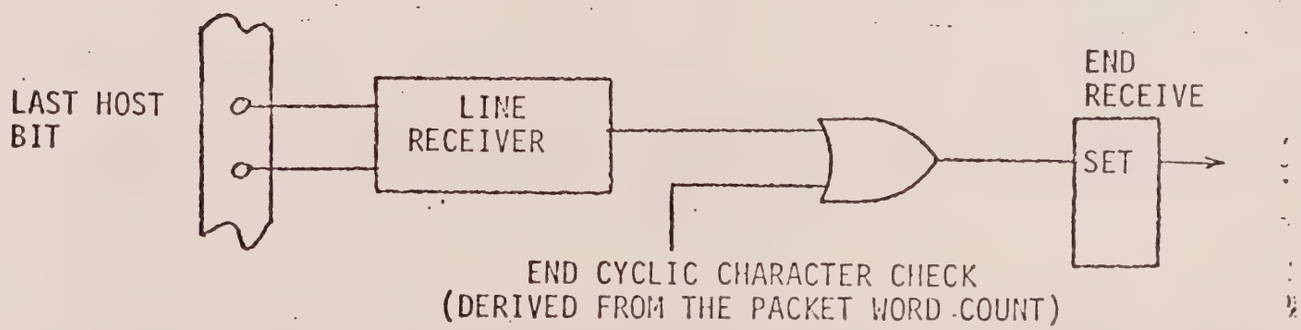


3.4 Last-Host Bit

The Last-Host bit will be or'ed with an internal signal that defines the last cyclic check code bit as derived by counting down the count in the packet count length field. This implementation will result in the following possibilities:

1) If the two cyclic code words are appended to the end of the packet and the Last-Host bit occurs on the last bit of the second cyclic code word, the receive interface card will check the cyclic code words. In this mode, the Last-Host bit basically has no effect on the receive operation.

2) If the cyclic code is not appended to the end of the packet, then the Last-Host bit will occur on the last bit of the last packet data word. In this mode, the Last-Host bit will cause the receive control to shut down without performing an error check.



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3.5 Ready Signals

3.5.1 PRU Master & Host Ready Test

A relay contact will be provided to accommodate these signals as defined in BB&N Report No. 1822. This relay will be under control of the PRU program via a control bit on the station transmit DMA channel.

3.5.2 Host Master Ready

The Host Master Ready Line will be gated with signals from the Host to prevent false interpretation of these signals. This signal will also be returned to the packet radio's processor program via the DMA status register.

3.5.3 Host Ready Test

This signal will be generated to test the condition of the Host via the Host Master Ready Line.

4.0 STATION CPU/PRU INTERFACE CONNECTIONS

Following is a summary of the signals on the Station CPU/PRU Interface. See Figure 4.0 for the interface cable diagram.

4.1 PRU Master Ready

The return for the PRU Ready Test signal through the (PRU) relay contact.

4.2 PRU Ready Test

The test signal sent to the packet radio to interrogate its ready status through the PRU relay contacts. No more than 100 mamp should flow in this wire and the PRU Master Ready wire.

4.3 Host Master Ready

The return for the Host-Ready-Test signal through the station CPU relay contact.

4.4 Host Ready Test

The ground signal sent to the station CPU to interrogate its ready status through the station CPU's relay contacts. No more than 100 mamp should flow in this wire and the Host Master Ready wire.

4.5 Host-to-PRU Data Line

The data from the station CPU should be changed for successive bits only after the PRU Ready-For-Next-Host-Bit signal goes off indicating that the previous bit has been accepted.

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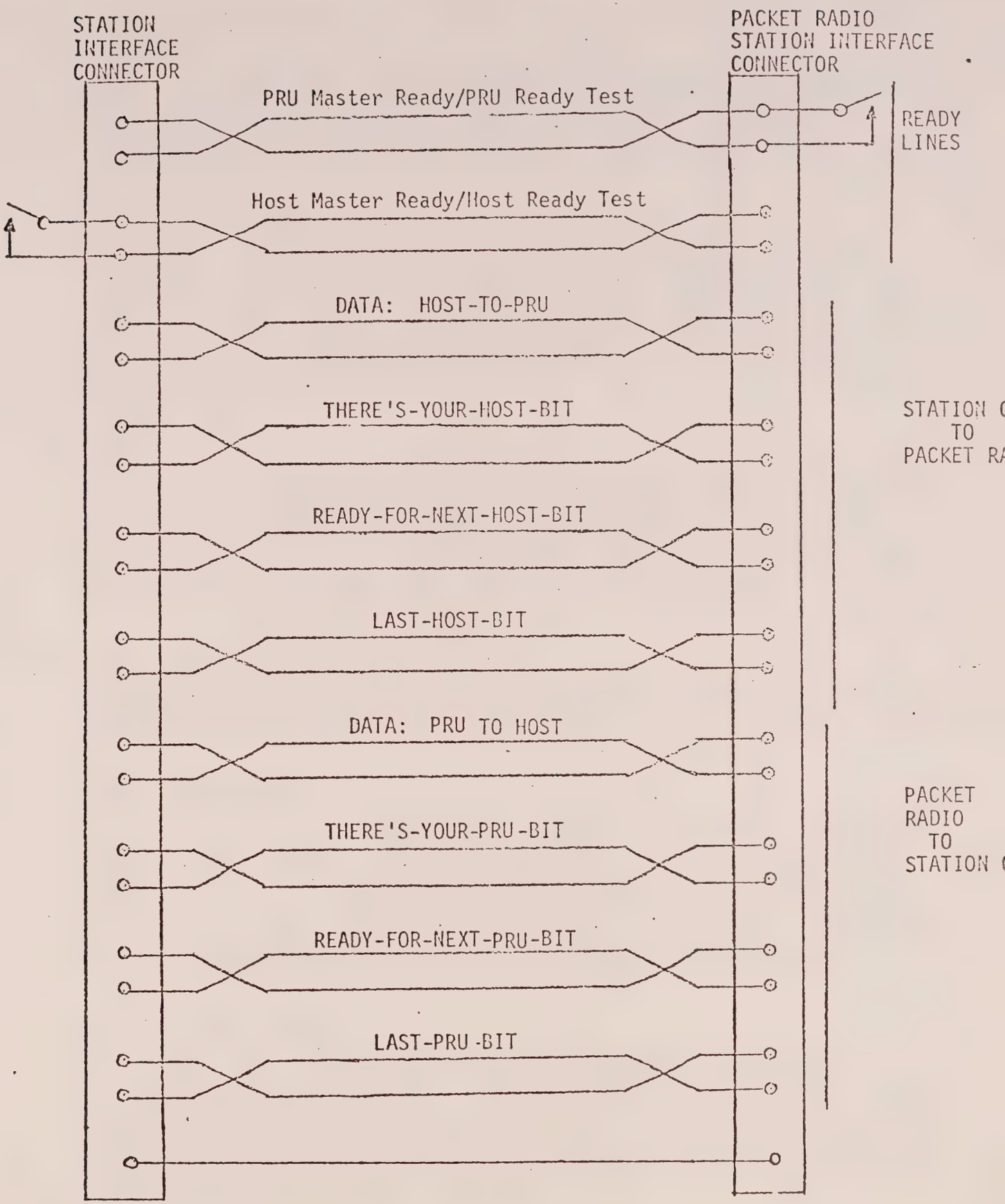
FIGURE 4.0: INTERFACE CABLE DIAGRAM



4.6 There's-Your-Host-Bit

This signal should be presented to the PRU by the station CPU as soon as the station CPU has a bit available to transmit and the PRU is indicating that it is Ready for Next Host Bit. When the Ready-For-Next-Host-Bit signal goes off, the There's-Your-Host-Bit signal should be removed.

4.7 Ready-For-Next-Host-Bit

This signal will be presented to the station CPU whenever the PRU is waiting for a transmission from the station CPU. Each time that the station CPU gives the PRU a bit (via There's-Your-Host-Bit), the Ready-For-Next-Host-Bit will go off after the bit has been taken in. It will go back on following an adjustable time delay (500 ns to 10 ns) after There's-Your-Host-Bit goes off.

4.8 Last-Host-Bit

When the station CPU transmits the last bit of a message, the Last-Host-Bit signal should be sent to the PRU in conjunction with the There's-Your-Host-Bit signal. Specifically, the Last-Host-Bit signal must come on no later than the There's-Your-Host-Bit signal comes on, and should remain on at least until Ready-For-Next-Host-Bit goes off. The Last-Host-Bit must occur on the 16th bit of the last word.

4.9 PRU-to-Host Data Line

The data for the station CPU will be changed for successive bits only after the Host's Ready-For-Next-PRU Bit goes off, indicating that the previous bit has been accepted.

4.10 There's-Your-PRU-Bit

This signal will be presented to the station by the PRU as soon as the PRU has a bit available to transmit and the station CPU presents the Ready-For-Next-PRU-Bit signal. When the Ready-For-Next-PRU-Bit goes off, the There's-Your-PRU-Bit signal will be removed. It will not be renewed until a new Ready-For-Next-PRU-Bit signal arrives. There will be a minimum of 500 ns delay in There's-Your-PRU-Bit going on following the PRU-to-Host Data Line becoming true for deskewing purposes.

4.11 Ready-For-Next-PRU-Bit

This signal should be presented to the PRU whenever the station CPU is ready to receive a new bit. Each time that the PRU gives the station a bit (via the There's-Your-Bit line), the Ready-For-Next-PRU-Bit signal go off after the bit has been taken in. This notifies the PRU that the bit has been taken and that a new bit can be placed on the PRU-to-Host Data Line. Ready-For-Next-PRU-Bit should be off at least until There's-Your-PRU-Bit goes off.

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4.12 Last-PRU-Bit

When the PRU transmits the last bit of the second cyclic check character the Last-PRU-Bit signal will be sent to the station CPU in conjunction with the There's-Your-PRU-Bit signal. Specifically, the Last-PRU-Bit signal will come on no later than the There's-Your-PRU-Bit signal, and will remain on until the station CPU turns off Ready-For-Next-PRU-Bit.

5.0 I/O INTERFACE LEVELS

BB&N Report No. 1822 defines two types of electrical interfaces, one using single ended devices and terminators and the other using differential drivers and terminators for use where the units may be physically separated by fairly long distances (up to 2000 ft.). The differential type interface was selected for use in the PRU Station Interface because this type of interface can handle both applications (local and distant).

The interface levels of plus and minus one volt centered around ground defined by BB&N Report No. 1822 are difficult to generate using available integrated circuits and the presently defined power voltages in the packet radio. The interface circuits described below, while not generating the exact voltages defined by BB&N Report No. 1822, are compatible with the driver/terminator circuits shown in Appendix D of Report No. 1822. The use of these circuits allows considerable savings in both power and circuit board real estate when compared to the circuits described in Report 1822.

5.1 I/O Line Receiver

The line terminator chosen for the PRU Station Interface is the DM7820 dual line receiver made by National Semiconductor Corporation. The unit has a differential input with a TTL output. The circuitry has input sensitivity of better than +0.2 volts with common mode interference of up to ±20 volts. The input resistance of the non-inverting input is 2.5K to ground while the input resistance of the inverting input is 5K to ground.

5.2 I/O Line Driver

The DM7830 dual line driver, along with level shifting interface resistors, was chosen as the line driver for the PRU Station Interface. The circuit is shown in Figure 5-2.

The output of this circuit is a differential voltage of ±1 volt. The output is centered around +0.5 volts as opposed to 0 volts defined by Report 1822. This results in a common mode signal of 0.5 volts presented to the line terminators specified by Report 1822. This common mode signal will be rejected by these terminators, thus making the signals defined for the PRU Station Interface compatible with those defined by BB&N Report No. 1822.

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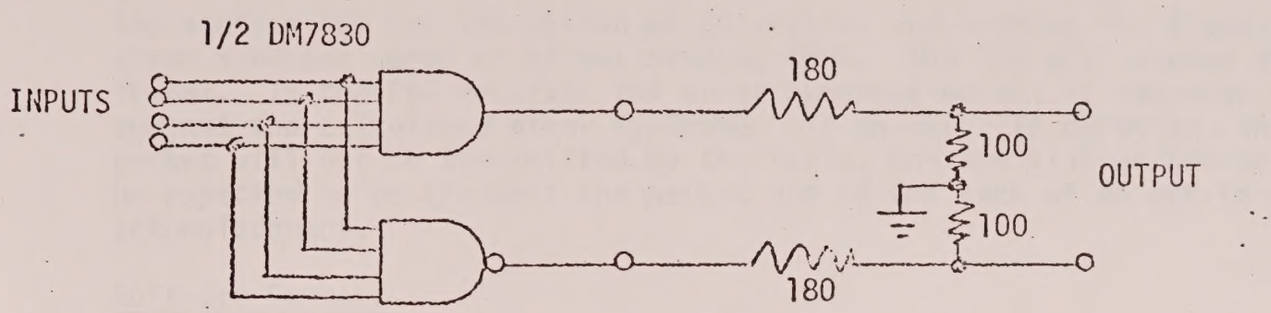

Figure 5.2

6.0 SOFTWARE OPERATIONS AND PROTOCOL

6.1 PRU Transmit to Station CPU

For the initial tests the software will be configured to transmit a packet to the Station CPU consisting of the following:

1) Packet Header (1 word)
2) Text (up to 126 words)
3) Received Error Syndrome (2 words)
4) Contents of the Receive Status Register (1 word)

In addition, the PRU station interface will add two additional error syndrome words covering the contente defined above.

The station CPU should be programmed to receive 132 words. The station CPU can determine the actual message length, following receive completion by inspecting the count field in the packet header.

If an error is detected by the PRU during transmit, either due to a transaction time out or to the station CPU dropping ready, the packet will be retransmitted to the station CPU. Once the PRU has transmitted the complete packet to the station CPU, the packet buffer in the PRU will be reallocated for another packet.

6.2 PRU Receive From Station's CPU

Whenever the PRU has packet buffer space available, it will enable its receive from station DMA channel to receive a packet. The packet from the station CPU must contain the count of the header plus text words in the first word of the packet header. The first word of the packet header must have this word count in bits 6 through Ø inclusive where bit 6 is the MSB. This is a hardware constraint.

The station CPU has the option of generating and sending the 2 additional error syndrome words or of not sending them. The PRU will accept either format. If the PRU receives the error syndrome words, it compares them against the calculated error syndrome. If an error is detected, the packet will not be transmitted by the radio, and the station CPU will be expected to re-transmit the packet due to the lack of an end-to-end acknowledgment.

6.3 Software Summary

The PRU will retransmit packets transmitted to the station CPU when errors are detected during the transmit process. It will discard packets with errors detected during receive from the station CPU. The PRU will not generate or receive positive acknowledge (ACK) or negative acknowledge (NAK) packets for packet transfer verification across the interface. The error rate across the interface is expected to be very low and thus the overhead imposed on the PRU for ACK, NAK of each packet is not deemed warranted. The rare loss of a packet should be determined and corrected by the end-to-end acknowledgment protocol.

The station has the option to check the error syndrome on packets received from the PRU and to generate the error syndrome on packets transmitted to the PRU.

If the error rate becomes significant across the station CPU/PRU interface an ACK/NAK protocol for each packet could be incorporated, or alternately, the hardware interface may be expanded to provide immediate acknowledgments and to resolve defined interface "lock-up" states.